Matthew San Jose

276 Fitzpatrick Hall, Notre Dame, IN 46556 | msanjose@nd.edu | (914) 806-7964

**Education**

**Ph. D in Electrical Engineering** August 2019 – August 2024

University of Notre Dame – Notre Dame, IN

GPA: 3.82/4.00

**Master of Science in Electrical Engineering** August 2019 – August 2021

University of Notre Dame – Notre Dame, IN

GPA: 3.81/4.00

**Bachelor of Science in Nanoscale Engineering**August 2015 - May 2019

State University of New York Polytechnic Institute – Albany, NY

*GPA:* 3.99/4.00

**Experience**

**Research Assistant** October 2019 - present

University of Notre Dame - Notre Dame, IN

* Designed, fabricated, and characterized non-planar silicon MOSFETs with a novel Zr-doped gate dielectric, demonstrating 20% greater drive current and 19% higher transconductance over control device
* Developed an improved TiN plasma etch recipe utilizing chlorine etchant rather than fluorine etchant, reducing etch time by 80%
* Reduced exposure time for source/drain lithography by 50% using a thinner, lower-dose resist while retaining sufficient masking capability for ion implantation
* Co-authored publications to IEEE conferences through collaborations with team members

**Clean Track Process Engineering Intern** August 2018 - July 2019

*Tokyo Electron (TEL) -* Albany, NY

* Performed cross-section SEM sample preparation and imaging of films and periodic structures with sub-micron dimensions
* Provided timely SEM images to assess experimental, 300 mm track-based approach for multiple patterning
* Reduced ellipsometer data workup time by over 90% with VBA macro
* Transferred cross-section SEM skills to previously untrained employee

**Thin Films Process Engineering Intern** May 2017- May 2018

*Tokyo Electron (TEL)* - Albany, NY

* Reduced deposition process time by 50% by installing heated chemical delivery system
* Upgraded multi-purpose vacuum system with various modifications, including increased temperature control and 66% expanded chemical capacity
* Collaborated with engineers, both within and outside of main group, to procure resources and expedite project completion
* Wrote and updated standard protocols for test equipment procedures

**Skills**

**Device fabrication:** process integration, reactive ion etching (RIE), electron-beam lithography (EBL), electron-beam evaporation, atomic layer deposition (ALD), projection lithography, DC sputtering, wet processing (e.g. HF treatments), chemical vapor deposition (CVD), backside wafer thinning

**Characterization:** current-voltage (IV) measurement, capacitance-voltage (CV) measurement, s-parameter measurement, scanning-electron microscopy (SEM), basic ellipsometry, x-ray photoelectron spectroscopy (XPS), focused-ion beam (FIB), cryogenic measurement

**Software:** MATLAB, Cadence Virtuoso Layout Suite, Visual Basic, ICCAP, ADS, Origin Pro

**Publications**

1. S. Dutta, B. Grisafe, C. Frentzel, Z. Encisco, **M. San Jose**, J. Smith, K. Ni, S. Joshi, S. Datta, “Experimental Demonstration of Gate-Level Logic Camouflaging and Run-Time Reconfigurability Using Ferroelectric FET for Hardware Security,” *IEEE Trans. Electron Devices*, vol. 68, no. 2, pp. 516–522, 2021, doi: 10.1109/TED.2020.3045380.
2. S. Dutta, H. Ye, W. Chakraborty, Y.-C. Luo, **M. San Jose**, B. Grisafe, A. Khanna, I. Lightcap, S. Shinde, S.Yu, S. Datta. “Monolithic 3D Integration of High Endurance Multi-Bit Ferroelectric FET for Accelerating Compute-In-Memory,” *2020 IEEE Int. Electron Devices Meet.*, vol. 1, no. c, pp. 801–804, 2020.
3. W. Chakraborty, **M. S. Jose**, J. Gomez, A. Saha, K.A. Aabrar, P. Fay, S. Gupta, S. Datta, “Higher-k Zirconium Doped Hafnium Oxide ( HZO ) Trigate Transistors with Higher DC and RF Performance and Improved Reliability,” *2021 Symp. VLSI Technol.*, vol. 47907, pp. T7-1, 2021.

**Presentations**

**Internal TEL Technical Seminar** May 2018

* Co-speaker for internal oral presentation about hardware and process developments from intern projects

**Summer Internship Symposium** August 2016

* Poster presentation to present results from organometallic photoresist precursor research

**Additional Experience**

**Equipment Engineering Intern** May - August 2018

*Maxim Integrated* – Beaverton, OR

* Improved safety of maintenance procedures for 12 etch tools for 6-inch wafer tools by designing lift assists for unwieldy parts over 35 lbs
* Created prototype for low-profile 75 lbs turbopump lift assist to make replacements safer

**Undergraduate Research Assistant**              September 2016 - May 2017

State University of New York Polytechnic Institute – Albany, NY

* Tested low-energy electrical response of photoresist thin-films for optimization of next-generation semiconductor device manufacturing processes
* Over 70% increased productivity by configuring automatic data acquisition from a previously manual acquisition set-up

**Summer Research Intern** June 2016 - August 2016

State University of New York Polytechnic Institute - Albany, NY

* Synthesized precursors to novel organometallic materials for better optimized EUV photoresists
* Handled flammable and air-sensitive chemicals (e.g. solvents, Grignard & organolithium reagents)
* Characterized samples using proton FT-NMR