Suman Datta

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Biography

Suman Datta received the B.Tech degree in Electrical Engineering from the Indian Institute of Technology, Kanpur, India and the Ph.D degree in Electrical and Computer Engineering from University of Cincinnati, Cincinnati, Ohio. He is the Stinson Chair Professor of Nanotechnology in the Department of Electrical Engineering at the University of Notre Dame, Notre Dame, Indiana, where he directs research in the Nanoelectronic Devices and Circuits Laboratory. He is also the Director of the $40.4M SRC/DARPA sponsored Applications and Systems-driven Center for Energy-efficient integrated NanoTechnologies (ASCENT). In addition, he is also the Director of the SRC/NSF sponsored Center for Extremely Energy Efficient Collective Electronics (EXCEL). His research involves brain-inspired computing, high performance general-purpose computing and collective state computing with CMOS and beyond CMOS devices. Prior to Notre Dame, he was a Professor of Electrical Engineering at The Pennsylvania State University, University Park, from 2007 to 2011. From 1999 till 2007, he was in the Advanced Transistor Group at Intel Corporation, Hillsboro, where he developed multiple generations of high-performance logic transistor technologies including high-k/metal gate, Tri-gate (FinFET) and non-silicon channel CMOS transistors.

Prof. Datta has co-authored 11 book chapters and over 380 refereed journal and conference papers, holds 185 patents and has presented numerous invited and keynote talks. His work has won 3 best paper awards (DRC 2010 and 2011, VLSI Symposium 2020), best paper nominations (IEDM 2016, 2018) and received over 25,265 citations (*h-index = 82*). He is a recipient of the Intel Achievement Award (2003), the Intel Logic Technology Quality Award (2002), the Penn State Engineering Alumni Association (PSEAS) Outstanding Research Award (2012), the SEMI Award for North America (2012) and the PSEAS Premier Research Award (2015). Prof. Datta has chaired premier IEEE conferences (DRC and IEDM), and serves on the Technical Program Committee of various top-tier IEEE conferences (VLSI Technology Symposium, IRPS etc.). In 2013, he was named Fellow of the Institute of Electrical and Electronics Engineers (IEEE) *for his contributions to high-performance advanced silicon and compound semiconductor transistor technologies*. In 2016, he was named Fellow of the National Academy of Inventors (NAI) *in recognition of his inventions that have made a tangible impact on quality of life, economic development and the welfare of society*.

Education

PhD, Electrical and Computer Engineering Dept., University of Cincinnati, OH, September 1999

Bachelors, Electrical Engineering Dept., Indian Institute of Technology, Kanpur, India, June 1995

Experience

Stinson Endowed Chair Professor (2015 – Present)

Department of Electrical Engineering, University of Notre Dame, IN

Director, Applications and Systems Driven Center for Energy-Efficient NanoTechnology (2018-Present)

DARPA/ SRC supported multi-university $40.4M center with 29 PIs, 14 schools, 120 researchers

Director, Center for Extremely Energy-Efficient Collective Electronics (2016 - Present)

NSF/ SRC supported multi-university $4.49M center with 10 PIs, 5 schools, 15 researchers

Professor (2011 – 2015)

Department of Electrical Engineering, Penn State University, PA

Monkowski Associate Professor (2007-2011)

Department of Electrical Engineering, Penn State University, PA

Principal Engineer (2005-2007)

Logic Technology Development, Intel Corporation, Hillsboro, OR

Senior Staff Engineer (2003-2005)

Logic Technology Development, Intel Corporation, Hillsboro, OR

Staff Engineer (2002-2003)

Logic Technology Development, Intel Corporation, Hillsboro, OR

Senior Process Engineer (1999-2002)

Logic Technology Development, Intel Corporation, Hillsboro, OR

Technology CAD (TCAD) Engineer (1999)

Avanti Corporation (now Synopsis), Fremont, CA

Technology Consultant (2008 – 2017)

TSMC (Taiwan Semiconductor Manufacturing Corp)

UMC (United Microelectronics Corp)

Samsung Electronics

Atomera

Research Career

Funded Projects (Total: $84M; Candidate's Share: $16M)

NRI

- Energy Efficient Transistor and Architectures, (06/08-05/11)- Phase 1, **Nanoelectronics Research Institute/Semiconductor Research Corporation (NRI/SRC)**, $525,920 (Total: $873,920 including PSU match of $348,000), (PI with T. Mayer, V. Narayanan, D. Schlom)(40% share)
- Energy Efficient Transistor and Architectures, (06/11 – 12/12) - Phase 1.5, **Nanoelectronics Research Institute/Semiconductor Research Corporation (NRI/SRC) and National Institute of Standards and Technology (NIST)**, $280,000 (PI with T. Mayer)(50% share)
- E2CDA: Extremely Energy Efficient Collective Electronics, (10/16 – 8/31), **National Science Foundation** (NSF) and **Semiconductor Research Corporation** (SRC), $4,290,000 (Center Director and PI) (Candidate's share $430,000

NSF

- Ultra-sensitive Magnetic Sensors Integrating the Giant Magnetoelectric Effect with MEMs and Advanced Microelectronics, (10/08-9/11), **National Science Foundation/Division of Electrical, Communications and Cyber Systems (NSF/ECCS)**, $352,273 (Co-PI with Q. Zhang (PI), EE, PSU and Q. Yang, Radiology, PSU Hershey Medical Center)(50% share)
- EMT/NANO:Co-Exploration of Device and System Architecture for Quantum NanoElectronics," (09/08-08/11), **National Science Foundation/Division of Computing and Communication Foundation (NSF/CCF)**, $200,020 (Co-PI with V. Narayanan (PI), EE, PSU)(50% share)
- Collaborative: Mixed Anion and Cation Based Transistor Architecture for Ultra-Low Power Complementary Logic Applications, (10/10-09/13), **National Science Foundation/ Division of Electrical, Communications and Cyber Systems (NSF/ECCS)**, $472,753 (PI with M. Hudait, EE, Virginia Tech)(50% share)
- MRSEC: Center for Nanoscale Science Supplement titled "Very Low Energy Dissipation Computing using Inter-band Tunneling Injected Non-equilibrium Ballistic Carriers," (10/10-09/13), **National Science Foundation/Nanotechnology Research Initiative** (NSF/NRI), $300,000, (Co-PI with T. Mayer(PI), EE, PSU)(50% share)
- ERC: NSF Nanosystems Engineering Research Center (NERC) for "Advanced Self-Powered Systems of Integrated Sensors and Technologies (ASSIST)," (10/12 – 09/19), **National Science Foundation,** $18,500,000 **(**Co-PI and Low Power Nanoelectronics Theme Leader)(Candidate's share $600,000 to date)
- EXPEDITION: NSF Expedition in Computing for "Visual Cortex on Silicon," (10/13 – 09/18), **National Science Foundation,** $10,000,000 **(**Low Power Nanoelectronics Theme Leader)(Candidate's share $500,000)
- EFRI 2DARE: Ultra-Low Power, Collective-State Device Technology Based on Electron Correlation in Two-Dimensional Atomic Layers, (9/13 – 12/17), **National Science Foundation,** $2,000,000 **(**Co-PI)(Candidate's share $500,000)
- MRSEC: Center for Nanoscale Science," (10/13-09/16), **National Science Foundation** (NSF), $18,300,000, (Senior Personnel) (Candidate's share $250,000)
- SemiSynBio: Cardiac Muscle-Cell-Based Coupled Oscillator Networks for Collective Computing (07/18 - 06/21), **National Science Foundation (NSF**), $1,125,000 (Co-PI) (Candidate's share $300,000)
- 2D Defect Zoology, Functionalization, and Application**, National Science Foundation (NSF)** (04/18 - 9/19), $75,000 (Candidate's share 100%)

DARPA, NSA, ONR, NIST, DTRA, SRC

- Mixed Anion Arsenide-Antimonide Channel Transistors with High-k Gate Stack, (11/09-10/12) **Semiconductor Research Corporation and Defense Advanced Research Projects Agency (SRC/DARPA),** $226,000 (PI)
- Architecture-Device Co-Design for Ultra-Low Power High Performance Design, (10/09-09/11), **National Security Agency (NSA),** $600,000 (Co-PI with V. Narayanan, EE, PSU)(50% share)
- Correlated Electron Switching Based Tunnel Transistors, (7/11-6/15), **Office of Naval Research** (ONR), $1,923,700 (PI with V. Gopalan, R. Engel-Herbert, MSE, PSU, D. Schlom, MSE, Cornell, K. Rabe, Physics, Rutgers)(25% share)
- Development and Demonstration of Next Generation Electronic Warfare Components based on Graphene Technologies, (01/02/12 – 12/31/14), **Office of Naval Research (ONR)**, $1,280,030 (Co-PI with J. Robinson, Electro-optic Center, PSU)(33% share)
- Ultrafast Spectroscopy in Heterojunction Tunnel Transistors, (10/11 – 9/13), **National Institute of Standards and Technology (NIST),** $120,000 (PI)
- Basic Single-Event and Total-Ionizing Dose Mechanisms in Antimony (Sb)-based CMOS Transistors with High-K Dielectric, (4/01/14-3/31/17), **Defense Threat Reduction Agency (DTRA)**, $1,745,560 (PI with D. McMorrow, NRL, K. Saraswat, EE, Stanford U.)(33% share)
- Architecture-Device Co-Design for Ultra-Low Power High Performance Design- Phase 2, (10/12-09/14), **National Security Agency (NSA),** $600,000 (Co-PI with V. Narayanan, EE, PSU)(50% share)
- Center for Low Energy Systems (LEAST) FCRP with Notre Dame Univ. (01/13-12/17) **Semiconductor Research Corporation and Defense Advanced Research Projects Agency (SRC/DARPA)** (total center funding is $ 30,000,000), Candidate is PI and Theme Leader for the "Quantum Engineered Steep Slope Transistors" $ 4,000,000 (over 5 years) (25% share)
- Oxide-based Reconfigurable Single-Electron Logic for Beyond CMOS, (10/13 - 9/14) **(Semiconductor Research Corporation**/Sematech) $62,125 (PI)
- Basic Single-Event and Total-Ionizing Dose Mechanisms in GE/InGaAs-based CMOS Transistors with ALD High-k Dielectric, (09/14 – 08/17) **Defense Threat Reduction Agency (DTRA)**, $1,045,560 (PI with C. Cress, NRL, K. Saraswat, EE, Stanford U.)(33% share)
- Landau FET Using Mott Hubbard Phase Transition, (1/14 - 12/17) **(Semiconductor Research Corporation**) $325,000 (PI)
- Ferroelectric Field Effect Transistor with Steep Switching Slope and Non-Volatile Functionality, (1/16 – 12/18) **(Semiconductor Research Corporation**) $300,000 (PI)
- Orbital Ordering Driven Threshold Switches for Select Devices in 3D X-Point Memories (11/15 – 10/17) **Semiconductor Research Corporation and Defense Advanced Research Projects Agency**

(SRC/DARPA) $ 500,000 (PI with S. Gupta, Penn St, and S. Guha, University of Chicago)(50% share)

- ASCENT - Applications and Systems driven Center for Energy-Efficient Integrated NanoTechnologies (01/18 - 12/22) **DARPA / Semiconductor Research Corporation** $ 38,386,478 (Director and Center Leader) (Candidate's share: $1,200,000)
- IMPACT - Innovative Materials and Processes for Accelerated Compute Technologies (IMPACT) Research Center (01/20 – 12/22) **DARPA / Semiconductor Research Corporation** $ 6,000,000 (PI) (Candidate's share: $1,000,000)
- Multi-Bit-per-Cell (MBC) Ferroelectric FET Memory Using Ferroelectric (FE) Superlattice with Anti-Ferroelectric (AFE) Interfacial Coupling, (1/20 – 12/22) **(Semiconductor Research Corporation**) $255,000 (PI)
- Multi-Component Semiconducting Oxide FETs: Materials-Device Co-Design, Synthesis, NanoFabrication, Characterization and Benchmarking, (1/20 – 12/22) **(Semiconductor Research Corporation**) $255,000 (PI)
- **T-MUSIC**: Negative Capacitance Enabled Scaling to Achieve 1 THz Cut-off Frequency Transistors on a CMOS Platform, (0/19 – 3/21) **(DARPA) $**444,302 (PI)
- **IIRM-URA**: Interaction with Ionizing Radiation with Matter, University Research Alliance (IIRM-URA) (07/20 – 12/24) **(DTRA)** $1,872,523 (PI)

Industry

- Compound Semiconductor Based Heterojunction Tunnel Transistors for Ultra Low Power Logic Applications-Phase 2, (09/01/09-08/31/12), **Intel Corporation**, $255,000 (PI)
- Ultra-Low Resistance Ohmic Contacts for III-V Digital Logic, (04/01/09-05/01/11), **Intel Corporation**, $250,000 (Co-PI with S. Mohney, Mat. Sc., PSU)(50% share)
- Post CMOS circuits and architecture, (10/01/10-09/30/13), **Academic Research Office (ARO), Intel Corporation**, $170,000 (PI)
- Sub-0.4V Logic Circuits with Steep Sub-threshold Slope Inter-band Tunnel FETs-Phase 2, (06/09-06/11) **Intel Corporation**, $70,000 (PI)
- Supply voltage scalability of III-V based heterojunction tunnel transistors -Phase 1, (09/08-08/09), **Intel Corporation**, $85,000 (PI)
- Multi-Gate III-V QWFET , (3/1/11-2/28/14), **Global Foundries**, $165,000 (PI)
- Germanium and III-V Devices, (08/11 – 07/12), **Applied Materials (AMAT)**, $ 60,000 (PI)
- Ultra Low Resistivity Metal Insulator Semiconductor (MIS) Contacts, (10/12 – 09/13), **Applied Materials** (AMAT), $ 60,000 (PI)

- Reliability Assessment of Highly Scaled High-k Gate Stacks, (10/12 – 09/13**), Applied Materials** (AMAT), $ 60,000 (PI)
- Variation Study of 3D Transistors, (10/11 – 09/14), **Lam Research**, $ 75,000 (PI)
- III-V-based Nanowire MOSFET and NanoPillar Tunnel FET for Ultra Low-Power Nanoelectronics, (2/12 – 07/15), **Samsung GRO**, $ 240,000 (PI)
- Ultra-scaled III-V FinFETs for Next Generation Nanoelectronics (11/15 – 1/17), **Samsung Electronics**, $ 120,000 (PI)
- 5nm Node Logic Transistor Option for Mobile System on a Chip ("SOC") (2/16 – 1/17), **Qualcomm**, $ 50,000 (PI)
- Low Voltage, High Non-Linearity (High ION & Low IOFF) Select Devices for Cross-point Memory Applications (06/17 - 05/20), **Intel Corporation**, $300,000 (PI)
- Functional Oxide based Cross-point Resistive Devices for Deep Neural Networks (04/17 - 04/19) **IBM Corporation**, $60,000 (PI)
- Investigation of Oxygen Insertion Channel Field Effect Transistor Architecture for Enhanced Transport and Improved Positive Bias Temperature Instabiliy (4/17 – 2/19) ATOMERA, $117,393 (PI)
- Transport in Gate-All-Around (GAA) Nanowire (NW) Transistors: Impact of NW Shape and Diameter (11/16 - 10/18), **Silicon Valley Community Foundation** $25,000 (PI)

Total number of publications to date:

– 385 total (**189 journal, 195 refereed conferences, 183 issued patents**)

– h-index = **82** with 25,265 citations (Google Scholar)

Total number of graduate students to date:

Postdoctoral: **10 completed**, **2 current**

PhD: **25 graduated** (including 2 IBM PhD Fellows, 1 Lam research PhD Fellow), **8 current**;

MS**: 8 graduated** (with thesis option), 0 current

Total number of issued United States patents: **183**

Graduated Students (25 PhDs, 9 Postdoctoral Researchers, 7 Masters)

1. Tanmoy Maiti (Postdoctoral Associate) (08/09-08/10) (Currently, Assistant Professor at Indian Institute of Technology, Kanpur, India)

2. Ramakrishnan Krishnan, PhD, 12/2009: Reliability Effects Of Soft Errors and NBTI in Current and Emerging Digital Circuits (Currently, Senior Staff Engineer, Advanced Technology Platforms Group, Taiwan Semiconductor and Manufacturing Corp (TSMC), Hsinchu, Taiwan)

3. Saurabh Mookerjea, PhD, 08/2010: Simulation, Design and Fabrication of Tunnel Transistors with steep sub-threshold slopes (Currently, Senior Device Engineer, Logic Technology Development, Intel Corporation, Hillsboro, Oregon)

4. Wei-Chieh Kao, MS (Thesis), 05/2010: Impact of Non-ideal Interfaces on Transistor Performance (Currently, PhD student at Arizona State University)

5. Vikram Sampat Kumar, MS (Thesis), 04/15/2010: An FPGA-based Real Time Tracking For Indoor Environment

6. Srijith Rajamohan, MS (Thesis), 04/2010: A Neural Network based Classifier on the Cell Broadband Engine

7. Ashkar Ali, MS (Thesis), 03/2009: Transport in Silicon Quantum Dots Embedded in a Rare Earth Oxide

8. Chad Ostrowski, BS (Honor's Thesis) 12/2009: Analytical Modeling of Tunnel Diodes

9. Vinay Saripalli, PhD, 10/31/11: Device Architecture Co-Design for Ultra Low Power Logic Using Emerging Tunneling Based Devices (Currently Senior CAD Engineer, Intel Corporation, Santa Clara)

10. Zhao Feng, PhD, 08/31/2011 : Ultra Sensitive Magnetic Sensors Integrating the Giant Magnetoelectric Effect with MEMS and Advanced CMOS (Currently Design Engineer, Texas Instruments, DallaS)
11. Salil Mujumdar, MS (Thesis), 05/2011: Strain Engineering in Nanoscale Transistors (Thesis option) (Current Device Engineer, Inter Molecular Foundry, San Jose)
12. Ashish Agrawal, MS (Thesis), 05/2011: Noise measurement and modeling of nanoscale devices (Thesis option) (Currently Ph.D. candidate at Penn State)
13. Ashkar Ali, PhD, 06/2012: Design and Fabrication of Ultra-low power and High Performance Quantum-well Transistors (IBM PhD Fellow 2010-2011, Currently Senior Device Engineer at Intel Corporation)
14. Feng Li, PhD, 08/2012: Ultra-sensitive Chip-Scale Magnetometers (Currently Design Engineer, Freescale Semiconductors)
15. Srinidhi Kestur, PhD, 01/2012: Accelerating computationally intensive applications using Reconfigurable systems (Currently Senior Design Engineer, Intel Corporation)
16. Euichul Hwang, PhD, 09/2012: Multi-gate III-V Metal Oxide Semiconductor FETs (Currently Device Engineer, Samsung Advanced Institute of Technology, SAIT)

17. Dheeraj Mohata, PhD, 01/2013: Arsenide-Antimonide Hetero-Junction Transistors for Low Power Logic Applications (Currently Integration Engineer, RF Micro Devices)

18. Ayan Kar, Post Doctoral Researcher, 02/13: (Currently Senior Device Engineer, Intel Corporation)

19. Eugene Freeman, MS (Thesis), 11/13: Correlated Electron Based Switches (Currently PhD student at Penn State)

20. Bijesh Rajamohanan: PhD, 05/2014: Fabrication, Characterization and Physics of III-V Tunneling Field Effect Transistors for Low Power Logic and RF Applications (Currently Senior Device Engineer, Sandisk Corporation)

21. Lu Liu: PhD, 05/2014: Classical and Coulomb Blockade III-V Multi-Gate Quantum Well Field Effect Transistors for Ultra Low Power Logic Applications (Currently Senior Device Engineer, Intel Corporation)

22. Ashish Agrawal: PhD, 12/2014: Physics and Technology of Strained Germanium Quantum Well FinFET for Low Power P-Channel Application (Currently Senior Device Engineer, Intel Corporation)

23. Huichu Liu: PhD, 5/2014: Circuit-Device Interaction for Steep Switching Slope Devices (Currently Senior Architecture Engineer, Intel Corporation)

24. Matt Hollander: PhD, 11/2015: Two-Dimensional Materials for Novel Elecctronic Applications: The Graphene Mixer and TaS_2 Hyper FET (Currently Senior Device Engineer, Micron Corporation)

25. Arun VT: PhD, 7/2015: Physics and technology of nanoscale III-V field effect transistors for low power electronics (Currently Senior Device Engineer, Intel Corporation)

26. Nidhi Agrawal: PhD, 7/2015: Numerical Simulation of Variation in 3D NonSilicon Transistors (Currently Senior Reliability Engineer, Micron Corporation)

27. Ali Razavieh (Post Doctoral Associate, PhD, Purdue University, West Lafayette, Indiana)(Currently, Senior Device Engineer, Global Foundries)

28. Bikas Das (Post Doctoral Associate, PhD, Indian Association of Cultivation of Science, Kolkata, India)(Currently Assistant Professor, IISER Calcutta)

29. Sandeepan Das Gupta (Post Doctoral Asssociate, PhD. Vanderbilt University)(Currently Senior Device Engineer, Micron Corporation)

30. Himanshu Madan: PhD, 12/2015: RF Electronics based on Emerging Devices (Currently Senior Device Engineer, Intel Corporation)

31. Mike Barth: Ph.D., 08/01/2016: Antimonide based Low Power Nanoelectronics (Currently Senior Process Engineer, Intel Corporation)

32. Rahul Pandey: Ph.D., 08/01/2016: Electrical Noise in Emerging Devices (Currently Senior Device Engineer, Intel Corporation)

33. Ramkrishna Ghosh (Post Doctoral Associate, PhD, Indian Institute of Science, IISc, Bangalore, India)(Assistant Professor, Jawarharlal Nehru University (JNU), Delhi, India)

34. Pankaj Sharma (Post Doctoral Associate, PhD, EPFL, Lausanne, Switzerland)(Currently Senior Process Integration Engineer, Micron Corporation)

35. Nikhil Shukla: PhD, 08/01/2017: Computational Device and Circuit Concepts using Electronic Phase Transition (Assistant Professor, ECE, University of Virginia, Charlottesville)

37. Xueqing Li (Post Doctoral Associate, PhD, Tsinghua University)(Assistant Professor, Tsinghua University, Beijing, China)

38. Matt Jerry: Ph.D.,10/01/2018: Collective Phenomena Based Solid State Devices and Their Natural Computing Applications (Senior Memory Array Engineer, Micron)

39. Kai Ni (Post Doctoral Associate, PhD, Vanderbilt University)(Assistant Professor, Rochester Institute of Technology, Rochester, New York, USA)

40. Benjamin Grisafe: Ph.D., 07/23/2020: Threshold Switching Phenomena and Their Application to Electronic Devices (Process Integration Engineer, Northrop Grumman)

41. Jeff Smith: Ph.D., 10/05/2020: Novel Silicon and Non-Silicon Transistors For Low Power Logic Applications

Current Research Interests

- Energy Efficient Beyond CMOS (e.g. negative capacitance transistors, phase transition transistors)
- Cryogenic FinFET CMOS (e.g. high performance compute)
- Monolithic 3D Integration (e.g. low temperature processed transistors)
- Intermittent computing with non-volatile memory (e.g. ferroelectric transistors)

- In-memory computing for machine learning accelerators (e.g. artificial neural networks using analog memory)
- Neuromorphic computing (e.g. spiking neural networks)
- Stochastic Computing (e.g. Ising solvers using probabilistic switching devices)
- Biocomputing (e.g. coupled oscillators using living heart muscle cells)

Awards and Honors

- Facebook Faculty Award (2020)
- Stinson Endowed Professorship (2019)
- Fellow of National Academy of Inventors (NAI) (2017) for "outstanding inventions that have made a tangible impact on quality of life, economic development and the welfare of society"
- Penn State Engineering Alumni Society (PSEAS) Premier Research Award (2015)
- IEEE Fellow for "contributions to for contributions to high-performance advanced silicon and compound semiconductor transistor technologies" (2013)
- SEMI Award for North America "in recognition of their pioneering work in the development, integration and introduction of a successful high-k dielectric and metal electrode gate stack for 45 nm CMOS IC production" (2012)
- IBM Faculty Award (2012)
- Penn State Engineering Alumni Society (PSEAS) Outstanding Research Award (2012)
- Distinguished Lecturer of IEEE Electron Devices Society (2011)
- Joseph Monkowsky Professorship for Faculty Early Career Development, The Pennsylvania State University (2007)
- Intel Achievement Award (the highest technical honor at Intel) for "developing the world's first high-K/metal gate CMOS transistors with record-setting performance" (2003)
- Divisional Achievement Award from Intel Logic Technology Development Group for "invention and successful demonstration of high performance Tri-gate CMOS transistors" (2002)
- All India Rank of 124 among 300,000 students who appeared for Indian Institute of Technology Joint Entrance Examination (IIT-JEE) (1995)

Research Supervision (current)

Postdoctoral Researcher (1)

- Sourav Dutta, PhD, Georgia Tech
- Navnidhi Upadhyay, PhD, University of Massachusetts, Amherst

Doctoral Students (8)

1. Fu-Xiang Liang: Analog In-Memory Computing (Start Date: 08/22/2020)

2. Sanjukta Banerjee: Ferroelectric Super-lattices for Analog Memory (Start Date: 08/22/2020)

3. Abhishek Khanna: Hardware for Unconventional Computing (Start Data: 07/01/2017)

4. Wriddhi Chakrobarty: Cryogenic High Performance Computing (Start Date: 08/22/2018)

5. Jorge Gomez: Bio-oscillators for Spatio-Temporal Signal Processing (Start Date: 08/22/2018)

6. Huacheng Ye: Sequential Monolithic Three dimensional Circuits (Start Date: 08/22/2018)

7. Matthew San Jose: Negative Capacitance FETs for TeraHertz Applications (Start Date: 08/22/2019)

8. Khandker Akif Aaabrar: Cryogenic Logic and Multi-bit per Cell Memory (Start Date: 05/01/2020)

MS Students (0)

None

Publications

Book Chapters

[1] V. Saripalli, V. Narayanan and S. Datta, "Ultra Low Energy Binary Diagram Circuits Using Few Electron Transistors", *Lecture Notes of the Institute for Computer Sciences, Social Informatics and Telecommunications Engineering*, Springer Berlin Heidelberg, October 2009

[2] V. Eachempati, R. Das, V. Narayanan, Y. Xie, S. Datta and C. Das, "HeTERO: Hybrid Topology Exploration for RF based On Chip Networks", *Communication Architectures for System-on-Chip (SoC),* CRC Press, September 2010

[3] S. Datta, D. Schlom, "Gate Oxides beyond SiO2", *Multifunctional Oxide Heterostructures*, Oxford University Press, September 2010

[4] S. Datta, "III-V MOSFETs", *Future Intelligent Integrated Systems: New Paths to Augmented Silicon CMOS Technologies*, WSPC-Pan Stanford (Singapore), January 2013

[5] Nikhil Shukla, S. Datta, A. Parihar, A. Raychowdhury, "Computing with Relaxation Oscillators*", Future Trends in Microelectronics*, Wiley, March 2016

[6] J. Robinson, M. Hollander, S. Datta, "Epitaxial Graphene: Progress on Synthesis and Device Integration", *2D Materials for Nanoelectronics*, CRC Press, May 2016

[7] Suman Datta, "Tri-Gate Transistors", *Nanoscale Silicon Devices*, CRC Press, Jan 2016

[8] Ahmedullah Aziz, Sumitha George, Xueqing Li, Suman Datta, Vijaykrishnan Narayanan, Sumeet Kumar Gupta, "Sensing in Ferroelectric Memories and Flip-Flops", *Sensing of Non-Volatile Memory Demystified*, Springer, Aug 2018

[9] Xueqing Li, Moon Seok Kim, Ahmedullah Aziz, Matthew Jerry, Nikhil Shukla, John Sampson, Sumeet Gupta, Suman Datta, Vijaykrishnan Narayanan, “Emerging Steep-Slope Devices and Circuits: Opportunities and Challenges”, *Beyond CMOS Technologies for Next Generation Computer Design*, Springer, Aug 2018

[10] Ahmedullah Aziz, Sandeep Krishna Thirumala, Danni Wang, Sumitha George, Xueqing Li, Suman Datta, Vijaykrishnan Narayanan, Sumeet Kumar Gupta, “Sensing in Ferroelectric Memories and Flip-Flops, *Sensing of Non-Volatile Memory Demystified*, Springer, 2019

Journal Articles

189] Y Hu, X Yao, DG Schlom, S Datta, K Cho "First Principles Design of High Hole Mobility p-Type Sn–O–X Ternary Oxides: Valence Orbital Engineering of Sn2+ in Sn2+–O–X by Selection of Appropriate Elements X" *Chemistry of Materials* Dec 2020

[188] W Chakraborty, H Ye, B Grisafe, I Lightcap, and S Datta "Low Thermal Budget (<250 °C) Dual-Gate Amorphous Indium Tungsten Oxide (IWO) Thin-Film Transistor for Monolithic 3-D Integration" *IEEE Transactions on Electron Devices* Vol, 67. No 12, pp 5336-5342 Nov 2020

[187] K Berggren, Q Xia, K K Likharev, D B Strukov,….., J Yang, K Roy, S Datta, and A Raychowdhury "Roadmap on Emerging Hardware and Technology for Machine Learning" *Nanotechnology* Vol 32 Issue 1 pp 012002 Oct 2020

[186] A Khan, A Keshavarzi, and S Datta "The Future of Ferroelectric Feld-effect Transistor Technology" *Nature Electronics* Oct 2020

[185] A Keshavarzi, K Ni, W Van Den Hoek, S Datta, and A Raychowdhury "FerroElectronics for Edge Intelligence" *IEEE Micro* Sept 2020

[184] M Si, J Andler, X Lyu, C Niu, S Datta, R Agrawal, and P Ye "Indium-Tin-Oxide Transistors with One Nanometer Thick Channel and Ferroelectric Gating" *ACS Nano* Aug 2020

[183] P Wang, Z Wang, X Sun, J Hur, S Datta, A Khan, and S Yu "Investigating Ferroelectric Minor Loop Dynamics and History Effect--Part II: Physical Modeling and Impact on Neural Network Training" *IEEE Transactions on Electron Devices*, DOI: 10.1109/TED.2020.3009956 Volume: 67 , Issue: 9 , Sept. 2020

[182] S Dutta, A Khanna, H Paik, D Schlom, A Raychowdhury, Z Toroczkai, and S Datta "Ising Hamiltonian Solver using Stochastic Phase-Transition Nano-Oscillators" arXiv preprint arXiv:2007.12331 Jul 24, 2020

[181] C Wu, H Ye, B Grisafe, S Datta and P Fay "Ferroelectric Polarization Switching Behavior of Hf0.5Zr0.5O2 Gate Dielectrics on Gallium Nitride High-Electron-Mobility-Transistor Heterostructures" *Physica Status Solidi* (a) https://doi.org/10.1002/pssa.201900717 April 2020

[180] S Dutta, C Shafer, J Gomez, K Ni, S Joshi, S Datta "Supervised Learning in All FeFET-Based Spiking Neural Network: Opportunities and Challenges" *Frontiers in Neuroscience* Jun 2020 DOI:10.3389/fnins.2020.00634

[179] A Kazemi, R Rajaei, K Ni, S Datta, M Niemier, XS Hu "A Hybrid FeMFET-CMOS Analog Synapse Circuit for Neural Network Training and Inference" arXiv preprint arXiv:2004.00703

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Recent Invited Talks (selected)

Universities

"Steep Slope Phase Transition FETs and their applications" École Polytechnique Fédérale de Lausanne EPFL, Lausanne, Switzerland, 1/2016

"Inter-band Tunnel Transistors: Opportunities and Challenges", *NEEDS Seminar*, Purdue University, West Lafayette, IN, 10/2015

"Negative Capacitance Ferroelectric Transistors: A Promising Steep Slope Device Candidate?", *NEEDS Seminar*, Purdue University, West Lafayette, IN, 10/2015

"Ultra Low Power Devices", *IEEE EDS Distinguished lecture series in Workshop on Connected, Autonomously Powered Systems,* Columbia University, New York, NY, 04/2014

"Cool Device Strategies for Beyond CMOS Nanoelectronics", *ECE Colloquium,* University of Texas, Dallas, TX, 02/2014

"Cool Device Strategies for Beyond CMOS Nanoelectronics", *ECE Colloquium,* Cornell University, Ithaca, NY, 02/2012

"Nanoelectronics for Future Energy Efficient Information Processing", *ECE Colloquium,* University of Illinois, Urbana Champagne, IL, 03/2012

"Tunnel Transistor Based Energy Efficient Logic", *IEEE EDS Distinguished lecture series in Electronics/Photonics,* Ohio State University, Columbus, OH, 04/2010

"Energy Efficient Logic Transistors using Compound Semiconductors" Cornell University Electron Devices Society Lecture Series, Cornell University, Ithaca, NY, 04/2010

"Logic and Memory Design using Inter-band Tunnel Transistor" Nanoseminar Seminar Series, Arizona State University, 03/2010

"Compound Semiconductor based Logic Elements" IEEE Electron Devices Mini Colloquium, Indian Institute of Technology, Mumbai, 01/2010

"Ushering in the Green Transistor Era", Rochester Institute of Technology, Rochester, New York, 5/2009

"Green Transistors to Green Architectures", Institut für Materialien und Bauelemente der Elektronik, Leibniz Universität Hannover (University of Hannover), Hannover, Germany, 10/2009

"Green Nanoelectronic Computing Devices", as part of the annual workshop on Emerging Trends in Photonic and Electronic Device Research held sponsored by The University of Illinois chapters of the Optical Society of America (OSA) and the IEEE Electron Devices Society (EDS) in conjunction with the Micro and Nanotechnology Laboratory (MNTL), University of Illinois, Urbana Champagne, Illinois, 09/2008

"Recent Advances in Silicon and Non-Silicon Nanoelectronic Devices for High-Performance, Energy Efficient Logic Applications", Penn State University Computer Science and Engineering Colloquia Series, 11/2007

"Emerging Nanoelectronic Devices for High-Speed and Ultra-Low Power Applications", sponsored by the University of Wisconsin, Madison, Materials Research Science and Engineering Center (MRSEC) in association with Electrical Engineering Department University of Wisconsin, Madison, Wisconsin, 12/2006

"Ultra Low Power Nanoelectronics for the Logic technology", Taipei Local Chapter of IEEE Electron Devices Society (EDS), National Tchao-tung University (NCTU), Hsinshu, Taiwan:, 12/2006

"Emerging Nanoelectronic Devices for High-Speed and Ultra-Low Power Application", Electrical Engineering Colloquium, University of Texas, Austin, 3/2006

"Silicon Nano-Transistors and Nanotechnology for High-Performance Logic Applications", sponsored by the IEEE Phoenix Section Components, Packaging, and Manufacturing Technology Society Chapter, & Waves and Devices Chapter, Arizona State University, Tempe, Arizona, 11/2003

Government/Industry

"Steep Slope Transistors", Speaker at the IEEE Rebooting Computing Workshop, Washington DC, 10/12/2015

"Steep Slope Transduction FETs", Invited Speaker at Global Foundries, Malta, New York, 10/21/2015

"Strained Germanium Quantum Well FinFETs", Invited Speaker at Global Foundries, Malta, New York, 09/01/2015

"Steep Slope Transistors", Keynote Speaker at the NSF sponsored "The Workshop for Energy Efficient Computing" Arlington, VA, 04/14/2015

"Function Stacks for Logic and Memory Devices", Invited Speaker at the SEMATECH's 7th International Symposium on Advanced Gate Stack Technology, in Albany, New York, 09/29/2010-10/01/ 2010

"Non silicon logic elements for extreme voltage scaling ", Invited Speaker at the IBM MRC Workshop on III/V Devices IBM Research, Zurich, Switzerland, 09/2010

"Binary Decision Diagram Logic for Single Electron Devices and Tunnel FETs", Invited Speaker at the Nanoelectronics Research Initiative (NRI) sponsored Architecture & Device Benchmarking Workshop, University of Notre Dame, 08/09/2010

"Tunnel Transistors: From Circuits to Architecture", Invited Speaker at the Nanoelectronics Research Initiative (NRI) sponsored Architecture & Device Benchmarking Workshop, University of Notre Dame, 08/09/2010

"High mobility channel MOSFETs: to include or not to include in the ITRS?", Panelist at the Sematech/IMEC III-V Workshop for discussion on inclusion high mobility channel MOSFETs in the ITRS, Hilton Hawaiian Village, Honolulu, 06/2010

"Green Transistors to Green Architectures", Tutorial at the 16th IEEE International Symposium on High-Performance Computer Architecture (HPCA), Bangalore, India, 01/2010

"High Mobility Channel MOSFETs", Panelist at the Workshop for Future III-V Complementary Metal–Oxide–Semiconductor (CMOS) Technology, Washington DC , December 2009

"Heterojunction Tunnel Transistor Logic," Intel on-site NRI sponsored PI's Workshop, Intel Corporation, Portland, Oregon, 8/2009

"Tunnel Transistor Logic", Intel Microprocessor Research Lab Seminar, Portland, Oregon, 10/09

"Looking Beyond Silicon - A Pipe Dream or the Inevitable Next Step?" Panelist on the IEDM sponsored evening panel called (This panel assembled internationally recognized panelists to discuss the future of Complementary Metal-Oxide Semiconductor (CMOS) and beyond CMOS for leading-edge advanced integrated circuit applications", 12/2007

"III-V Complementary Metal-Oxide Semiconductor (CMOS) on Si: Technical and Manufacturing Needs" Panelist on the Sematech and Aixtron sponsored workshop on readiness of III-V MOSFET Technology. This workshop received world-wide press coverage under the heading "III-V Compounds Emerging as Prime Materials for Future NMOS Channels, Technologists Indicate at SEMATECH & AIXTRON Workshop," Washington, D.C., 12/2007

Inventions

[184] US Patent # 10937907 "Method for fabricating transistor with thinned channel "

[183] US Patent # 10839880 "Low power sense amplifier based on phase transition material"

[182] US Patent # 10707319 "Gate electrode having a capping layer"

[181] US Patent # 10672475 "Nonvolatile digital computing with ferroelectric FET"

[184] US Patent # 10475514 "Nonvolatile digital computing with ferroelectric FET"

[183] US Patent # 10367093 "Method for fabricating transistor with thinned channel"

[182] US Patent # 10262714 "Low power sense amplifier based on phase transition material"

[181] US Patent # 10141437 "Extremely high mobility CMOS logic"

[180] US Patent # 10121897 "Field effect transistor with narrow bandgap source and drain regions and method of fabrication"

[179] US Patent # 9991172 "Forming arsenide-based complementary logic on a single substrate "

[178] US Patent # 9806195 "Method for fabricating transistor with thinned channel"

[177] US Patent # 9800094 "Low power nanoelectronics"

[176] US Patent # 9761724 "Semiconductor device structures and methods of forming semiconductor structures"

[175] US Patent # 9748391 "Field effect transistor with narrow bandgap source and drain regions and method of fabrication"

[174] US Patent # 9691856 "Extremely high mobility CMOS logic"

[173] US Patent # 9614083 "Field effect transistor with narrow bandgap source and drain regions and method of fabrication"

[172] US Patent # 9548363 "Extremely high mobility CMOS logic"

[171] US Patent # 9425256 "Strain inducing semiconductor regions"

[170] US Patent # 9391068 "Power rectifier using tunneling field effect transistor"

[169] US Patent # 9385180 “Semiconductor device structures and methods of forming semiconductor structures”

[168] US Patent # 9368583 “Gate electrode having a capping layer”

[167] US Patent # 9287380 “Field effect transistor with narrow bandgap source and drain regions and method of fabrication”

[166] US Patent # 9337307 “Method for fabricating transistor with thinned channel ”

[165] US Patent # 9287380 “Gate electrode having a capping layer”

[164] US Patent # 9048314 “Field effect transistor with narrow bandgap source and drain regions and method of fabrication”

[163] US Patent # 9006707 “Forming arsenide-based complementary logic on a single substrate”

[162] US Patent # 8841180 “Strain-inducing semiconductor regions”

[161] US Patent # 8816394 “Field effect transistor with narrow bandgap source and drain regions and method of fabrication”

[160] US Patent # 8803255 “Gate electrode having a capping layer ”

[159] US Patent # 8802517 “Extreme high mobility CMOS logic ”

[158] US Patent # 8664694 “Field effect transistor with narrow bandgap source and drain regions and method of fabrication”

[157] US Patent # 8638591 “TFET based 4T memory devices”

[156] US Patent # 8581258 “Semiconductor device structures and methods of forming semiconductor structures”

[155] US Patent # 8530884 “Strain inducing semiconductor regions”

[154] US Patent # 8518768 “Extreme high mobility CMOS logic”

[153] US Patent # 8421059 “Strain inducing semiconductor region”

[152] US Patent # 8405164 “Tri-gate transistor device with stress incorporation layer and method of fabrication ”

[151] US Patent # 8390082 “Gate electrode having a capping layer ”

[150] US Patent # 8369134 “TFET based 6T SRAM cell ”

[149] US Patent # 8368135 “Field effect transistor with narrow bandgap source and drain regions and method of fabrication”

[148] US Patent # 8294180 “CMOS devices with a single work function gate electrode and method of fabrication”

[147] US Patent # 8288233 “Method to introduce uniaxial strain in multigate nanoscale transistors by self aligned SI to SIGE conversion processes and structures formed thereby ”

[146] US Patent # 8273626 “Nonplanar semiconductor device with partially or fully wrapped around gate electrode and methods of fabrication”

[145] US Patent # 8264004 “Mechanism for forming a remote delta doping layer of a quantum well structure”

[144] US Patent # 8237234 “Transistor gate electrode having conductor material layer”

[143] US Patent # 8232588 “Increasing the surface area of a memory cell capacitor”

[142] US Patent # 8217383 “High hole mobility p-channel Ge transistor structure on Si substrate”

[141] US Patent # 8193567 “Process for integrating planar and non-planar CMOS transistors on a bulk substrate and article made thereby ”

[140] US Patent # 8183646 “Field effect transistor with narrow bandgap source and drain regions and method of fabrication ”

[139] US Patent # 8183556 “Extreme high mobility CMOS logic”

[138] US Patent # 8169027 “Substrate band gap engineered multi-gate pMOS devices”

[137] US Patent # 8148786 “Complementary metal oxide semiconductor integrated circuit using raised source drain and replacement metal gates”

[136] US Patent # 8138042 “Capacitor, method of increasing a capacitance area of same, and system containing same”

[135] US Patent # 8129795 “Inducing strain in the channels of metal gate transistors”

[134] US Patent # 8124959 “High hole mobility semiconductor device”

[133] US Patent # 8120065 “Tensile strained NMOS transistor using group III-N source/drain regions”

[132] US Patent # 8119508 “Forming integrated circuits with replacement metal gate electrodes”

[131] US Patent # 8084818 “High mobility tri-gate devices and methods of fabrication”

[130] US Patent # 8071983 "Semiconductor device structures and methods of forming semiconductor structures," J. Brask, J. Kavalieros, U. Shah, S. Datta, A. Majumdar, R. Chau, B. Doyle, Dec 06, 2011

[129] US Patent # 79892807 "Dielectric interface for group III-V semiconductor device," J. Brask, S. Datta, M. Doczy, J. Blackwell, M. Metz, J. Kavalieros, R. Chau, Aug 02, 2011

[128] US Patent # 7968957 "Transistor gate electrode having conductor material layer," A. Murthy, B. Boyanov, S. Datta, B. Doyle, B. Jin, S. Yu, R. Chau, June 28, 2011

[127] US Patent # 7960794 "Non-planar pMOS structure with a strained channel region and an integrated strained CMOS flow," B. Doyle, S. Datta, B. Jin, N. Zelick, R. Chau, June 14, 2011

[126] US Patent # 7951673 "Forming abrupt source drain metal gate transistors," N. Lindert, S. Datta, J. Kavalieros, M. Doczy, M. Metz, J. Brask, R. Chau, M. Bohr, A. Murthy, May 31, 2011

[125] US Patent # 7915694 "Gate electrode having a capping layer," G. Dewey, M. Doczy, S. Datta, J. Brask, M. Metz, Mar 29, 2011

[124] US Patent # 7915167 "Fabrication of channel wraparound gate structure for field-effect transistor," M. Radosavljevic, A. Majumdar, B. Doyle, J. Kavalieros, M. Doczy, J. Brask, U. Shah, S. Datta, R. Chau, Mar 29, 2011

[124] US Patent # 7902058 "Inducing strain in the channels of metal gate transistors," S. Datta, J. Kavalieros, M. Doczy, M. Metz, J. Brask, R. Chau, B. Doyle, Mar 08, 2011

[123] US Patent # 7902014 "CMOS devices with a single work function gate electrode and method of fabrication," B. Doyle, B. Jin, J. Kavalieros, S. Datta, J. Brask, R. Chau, Mar 08, 2011

[122] US Patent # 7898041 "Block contact architectures for nanoscale channel transistors," M. Radosavljevic, A. Majumdar, B. Doyle, J. Kavalieros, M. Doczy, J. Brask, U. Shah, S. Datta, R. Chau, Mar 01 , 2011

[121] US Patent # 7893506 "Field effect transistor with narrow bandgap source and drain regions and method of fabrication," R. Chau, S. Datta, J. Kavalieros, J. Brask, M. Doczy, M. Metz, Feb 22, 2011

[120] US Patent # 7888221 "Tunneling field effect transistor using angled implants for forming asymmetric source/drain regions," J. Kavalieros. M. Metz, G. Dewey, B. Jin, J. Brask, S. Datta, R. Chau, Feb 15, 2011

[119] US Patent # 7883951 "CMOS device with metal and silicide gate electrodes and a method for making it," J. Brask, M. Doczy, J. Kavalieros, M. Metz, C. Barns, U. Shah, S. Datta, C. Thomas, R. Chau, Feb 08, 2011

[118] US Patent # 7879739 "Thin transition layer between a group III-V substrate and a high-k gate dielectric layer," W. Rachmady, J. Blackwell, S. Datta, J. Kavalieros, M. Hudait, Feb 01, 2011

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[116] US Patent # 7875937 "Semiconductor device with a high-k gate dielectric and a metal gate electrode," M. Metz, M. Doczy, J. Brask, J. Kavalieros, R. Chau, Robert S, Jan 25, 2011

[115] US Patent # 7871916 "Transistor gate electrode having conductor material layer," A. Murthy, B. Boyanov, S. Datta, B. Doyle, B. Jin, S. Yu, R. Chau, Jan 18, 2011

[114] US Patent # 7859081 "Capacitor, method of increasing a capacitance area of same, and system containing same," B. Doyle, R. Chau, S. Datta, V. De, A. Keshavarzi, D. Somasekhar, Dec 28, 2010

[113] US Patent # 7858481 "Method for fabricating transistor with thinned channel," J. Brask, R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, A. Majumdar, M. Metz, M. Radosavljevic, Dec 28, 2010

[112] US Patent # 7825481 "Field effect transistor with narrow bandgap source and drain regions and method of fabrication," R. Chau, S. Datta, J. Kavalieros, J. Brask, M. Doczy, M. Metz, Nov 02, 2010

[111] US Patent # 7825437 "Unity beta ratio tri-gate transistor static random access memory (SRAM)," R. Pillarisetty, S. Datta, J. Kavalieros, B. Doyle, U. Shah, Nov 02, 2010

[110] US Patent # 7825400 "Strain-inducing semiconductor regions," S. Datta, J. Kavalieros, B. Jin, Nov 02, 2010

[109] US Patent # 7820513 "Nonplanar semiconductor device with partially or fully wrapped around gate electrode and methods of fabrication," S. Hareland, R. Chau, B. Doyle, R. Rios, T. Linton, S. Datta, Oct 26, 2010

[108] US Patent # 7820512 "Spacer patterned augmentation of tri-gate transistor gate length," R. Pillarisetty, S. Datta, J. Kavalieros, B. Doyle, U. Shah. Oct 26, 2010

[107] US Patent # 7791063 "High hole mobility p-channel Ge transistor structure on Si substrate," M. Hudait, S. Datta, J. Kavalieros, P. Tolchinsky, Sept 07, 2010

[106] US Patent # 7790536 8 "Dopant confinement in the delta doped layer using a dopant segregration barrier in quantum well structures" M. Hudait, A. Budrevich, D. Loubychev, J. Kavalieros, S. Datta, J. Fastenau, A. Liu Sept 07, 2010

[105] US Patent # 7785958 "Method for making a semiconductor device having a high-k gate dielectric layer and a metal gate electrode," M. Doczy, J. Brask, J. Kavalieros, U. Shah, M. Metz, S. Datta, R. Nagisetty, R. Chau, Aug 31, 2010.

[104] US Patent # 7776684 "Increasing the surface area of a memory cell capacitor," B. Doyle, R. Chau, V. De, D. Somasekhar, Aug 17, 2010.

[103] US Patent # 7736956 "Lateral undercut of metal gate in SOI device," S. Datta, J. Brask, J. Kavalieros, B. Doyle, G. Dewey, M. Doczy, R. Chau, June 15, 2010.

[102] US Patent # 7718479 "Forming integrated circuits with replacement metal gate electrodes," J. Kavalieros, J. Brask, M. Doczy, M. Metz, S. Datta, U. Shah, R. Chau, May 18, 2010.

[101] US Patent # 7714397 "Tri-gate transistor device with stress incorporation layer and method of fabrication," S. Hareland, R. Chau, B. Doyle, S. Datta, B. Jin, May 11, 2010.

[100] US Patent # 7713803 "Mechanism for forming a remote delta doping layer of a quantum well structure," B. Jin, J. Kavalieros, S. Datta, A. Majumdar, R. Chau, B. Jin, May 11, 2010

[99] US Patent # 7709909 "Method for making a semiconductor device having a high-k gate dielectric," M. Doczy, G. Dewey, S. Datta, S. Pae, J. Brask, J. Kavalieros, M. Metz, A. Sherrill, M. Kuhn, R. Chau, May 04, 2010.

[98] US Patent # 7704833 "Method of forming abrupt source drain metal gate transistor," N. Lindert, S. Datta, J. Kavalieros, M. Doczy, M. Metz, J. Brask, R. Chau, M. Bohr, A. Murthy, April 27, 2010.

[97] US Patent # 7671471 "Method for making a semiconductor device having a high-k dielectric layer and a metal gate electrode," J. Brask, J. Kavalieros, M. Doczy, U. Shah, C. Barnes, M. Metz, S. Datta, A. Cappellani, R. Chau, March 03, 2010.

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Professional Activities

Associate Editor, IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

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General Chair*, IEEE International Electron Devices Meeting (IEDM '20)*, San Francisco, December 2020

Chair*, Technical Program, IEEE International Electron Devices Meeting (IEDM '19)*, San Francisco, December 2019

Vice Chair*, Technical Program, IEEE International Electron Devices Meeting (IEDM '18)*, San Francisco, December 2018

Chair*, Short Course, IEEE International Electron Devices Meeting (IEDM '17)*, San Francisco, December 2017

Vice Chair*, Short Course, IEEE International Electron Devices Meeting (IEDM '16)*, San Francisco, December 2016

Chair, *Publications, IEEE International Electron Devices Meeting (IEDM '15)*, Washington DC, December 2015

TPC Member, Arrangements Chair, VLSI Technology Symposium **(***VLSI Symposium '19*), Honolulu, Hawaii

TPC Member, VLSI Technology Symposium **(***VLSI Symposium '18*), Kyoto, Japan

TPC Member, Design Automation Conference (DAC '16, DAC '17)

TPC Member, International Conference on Simulation of Semiconductor Processes & Devices (SISPAD '16), Dresden, Germany

TPC Member, International Reliability Physics Symposium (IRPS '16, IRPS '17)

Chair, *Publicity, IEEE International Electron Devices Meeting (IEDM '14)*, San Francisco, California, December 2014

Chair, *Tutorials, IEEE International Electron Devices Meeting (IEDM '12)*, San Francisco, California, December 2012

General Chair, *IEEE Device Research Conference (DRC)*, Notre Dame University, University Park, PA, June 2013

Program Chair, *IEEE Device Research Conference (DRC)*, Pennsylvania State University, University Park, PA, June 2012

Chair, *Emerging Technologies, IEEE International Electron Devices Meeting (IEDM '11)*, Washington DC, December 2011

TPC Vice-Chair, *IEEE Device Research Conference (DRC)*, University of California, Santa Barbara, CA, June 2011

Chair, *Quantum, Power, and Compound Semiconductor Devices Sub-Committee, IEEE International Electron Devices Meeting (IEDM '10)*, San Francisco, California, December 2010

Organizer and Chair, *Rump Session on Embedded Memory called "Looking for Extra Cache"*, *IEEE Device Research Conference (DRC '10),* Univ. of Notre Dame, June 2010

Organizer and Chair, *Rump Session on Steep Slope Transistors called "Steep Slope or Slippery Slope"*, *IEEE Device Research Conference (DRC '10),* Penn State University, June 2009

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TPC Member, *Semiconductor Interface Specialist Conference (SISC '10),* San Diego, California, December2010

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TPC Member, *Silicon Nanoelectronics Workshop (SNW '08)*, Honolulu, Hawaii, June 2008

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Panel Chair, *ACM/IEEE International Symposium Low Power Electronics and Design (ISLPED '09)*, San Francisco, California, August 2009

Session Chair, *"Non Volatile Memory" at the High-K Dielectric Materials and Gate Stack Symposium, Electrochemical Society Meeting (ECS '09),* Vienna, Austria, October 2009

Session Chair, *"MOS Devices" at the IEEE Device Research Conference (DRC '09), June 2009*

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Session Co-Chair, "III-V Logic Transistors with Advanced Gate Stack" at the *IEEE International Electron Devices Meeting (IEDM '09)*, Baltimore, Maryland, December 8, 2009

Session Co-Chair, *"Heterostructure High-Speed Devices"* at the *IEEE International Electron Devices Meeting (IEDM '08),* San Francisco, California, December 2008

Session Chair, *"Materials for Ge and Si devices"* at the *International Conference on Insulating Films on Semiconductors (INFOS '07)*, Athens, Greece, June 2007

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Nature Materials

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IEEE Electron Device Letters

ACM Journal on Emerging Technologies in Computing Systems

Solid-State Electronics

Applied Physics Letters

Journal of Applied Physics

Journal of Vacuum Science and Technology B

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Nanotechnology (Journal) from Institute of Physics (IOP)

Journal of Electronic Materials

ACS Nano

IEDM, DRC, ESSDERC, VLSI-TSA, IEEE ISLPED, SISC, EMC, IEEE SNW, VLSI Symposia on Technology and Circuits