WRIDDHI CHAKRABORTY
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SR 131 Stinson Remick Hall, University of Notre Dame, Notre Dame, IN 46556

EDUCATION

University of Notre Dame, Notre Dame, IN — August 2018 - Present
Ph.D. Candidate in Electrical Engineering
Thesis Advisor: Professor Suman Datta
Cumulative Grade Point Average: 3.72/4.00

Indian Institute of Engineering Science & Technology, Shibpur, India — August 2014 - May 2018
Bachelor of Technology in Electronics &Telecommunication Engineering
Cumulative Grade Point Average: 9.26/10.00, Departmental Rank: 2/40

PUBLICATIONS

Key Publications

- **W.Chakraborty**, B. Grisafe, H. Ye, I. Lightcap, K.Ni, and S.Datta, "BEOL Compatible Dual-Gate Ultra-Thin Body W-Doped Indium-Oxide Transistor with I_{ON}=370µA/µm, SS=73mV/dec and I_{ON}/I_{OFF} ratio >4x10^9", 2020 Symposium on VLSI Technology, Honolulu, HI ***(Best Student Paper Award)***

- **W. Chakraborty**, K. Ni, J. Smith, A. Raychowdhury and S. Datta, "An Empirically Validated Virtual Source FET Model for Deeply Scaled Cool CMOS", 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA

- **W.Chakraborty**, U. Sharma, S.Datta and S. Mahapatra, "Hot Carrier Degradation in Cool-CMOS", 2020 IEEE International Reliability Physics Symposium, Dallas, TX

- K. Ni, A.K.Saha, **W.Chakraborty**, H.Ye, B. Grisafe, J. Smith, G.B.Rayner, S.Gupta, and S.Datta, "Equivalent Oxide Thickness (EOT) Scaling with Hafnium-Zirconium Oxide High-K Dielectric near Morphotropic Phase Boundary" , 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA

- K. Ni, **W. Chakraborty**, J. Smith, B. Grisafe and S. Datta, "Fundamental Understanding and Control of Device-To-Device Variation in Deeply Scaled Ferroelectric FETs", 2019 Symposium on VLSI Technology, Kyoto, Japan

- K. Ni, B. Grisafe, **W. Chakraborty**, A. Saha, S. Dutta, M. Jerry, J. Smith, S. Gupta, S. Datta, "In-Memory Computing Primitive for Sensor Data Fusion in 28 nm HKMG FeFET Technology", 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA

- **W. Chakraborty**, R. Ray, N. Samanta, C. RoyChaudhuri, "Quantitative Differentiation of Multiple Virus in Blood using Nanoporous Silicon Oxide Immunosensor and Artificial Neural Network", Biosensors and Bioelectronics (Impact Factor: 7.780), Elsevier, 2017

ACADEMIC HONORS

- Recipient of Best Student Paper Award in VLSI Symposium for Technology and Circuits, 2020.
- Selected for DAAD-WISE Internship (2018) at Universität Bremen, Germany, awarded to 300 students in India
- Received Research Fellowship for excellence in undergraduate research (2018) and University Merit Scholarship for excellence in undergraduate studies (2018) from Global Alumni Association of Bengal Engineering and Science University, Shibpur (GAABESU).
- Ranked among top 0.33 % in All India Joint Entrance Exam (2014) and was among the top 100 rank-holders in state-level Higher Secondary Examination (2014).

RESEARCH EXPERIENCES

Emerging Memory Cell Team, Micron Technology, Boise, ID **June 2020-August 2020**
Summer Research Intern

- Evaluation of device reliability for DRAM access-transistors through charge-pumping technique
- Characterization of gate oxide-channel interface through Random Telegraph Noise (RTN) measurements for NAND array transistors

University of Notre Dame, Notre Dame, IN **June 2018-present**
Graduate Research Assistant

- **Cryogenic CMOS Technology for Next Generation Computing**

  - Evaluation of system level performance improvement in advanced node CMOS technologies (14nm FinFET, 22nm FDSOI) at cryogenic temperature (down to 4K), through device characterization and physics based compact model development.
  - Characterization of device reliability (NBTI, PBTI and Hot-Carrier Degradation) and developing physics based compact model to evaluate performance boosting and circuit-aging at cryogenic temperature
  - Evaluation of Power performance analysis in advanced node CMOS technologies at cryogenic temperature through Threshold Voltage adjustment

- **Back-end-of-the-line (BEOL) Compatible Oxide-Semiconducting FETs for Monolithic 3D application**

  - Experimental demonstration of Back-end-of-the-line compatible Amorphous Oxide Semiconductor transistors (Tungsten doped Indium-Oxide or IWO) with short channel length (50nm), ultra-high I_{ON}/I_{OFF} ratio (~10^{12}) and record I_{ON} (~550μA/μm) at V_{DD}=1V.
  - Investigation of Threshold Voltage Instability in Oxide-Semiconductor FETs under different processing conditions to identify and mitigate the origin of performance degradation maintaining device performance.

Undergraduate Research

Group of Computer Architecture, Universität Bremen, Germany **May 2017-July 2017**

- Developing algorithm for synthesising arbitrary complex Quantum Circuits (Q-circuits) with Clifford+T-basis group, with specific focus on Q-circuits with transformation matrices having complementary column entries and n-bit Quantum Fourier Transform Circuit.

INVITED TALKS

- **"High Performance Cryogenic-CMOS for Cold Computing"**
  VLSI-TSA Symposium, Hsinchu, Taiwan **to be held on April 2021**

- **"Cool-CMOS Technology for next generation High Performance Computing"**
  Microsoft Research, Redmond, WA. **June 2020**

TECHNICAL SKILLS

- **Electronic Device Characterization**
  MOSFET Reliability Measurements (NBTI/PBTI, Hot Carrier Degradation, Charge Pumping), Random Telegraph Noise (RTN) Measurements, Split-Capacitance Measurement, Transient Measurements for analysing Ferroelectric Polarization Switching in MFM Capacitor and FeFET, DC/Pulsed Current-Voltage (I-V), Capacitance-Voltage Measurement(C-V).

- **Simulations and EDA**
  MATLAB, LTspice, NI MultiSim, COMSOL Multiphysics